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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/009,842	12/17/2001	Kyoko Hirata	60188-131	1177

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/009,842	HIRATA ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on November 19, 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Santin et al. (US 5,815,026).

In re claim 1, Santin et al. shows (fig. 2a) a semiconductor device comprising a first conductive type semiconductor layer (14), at least one first unit cell including a first conductive type first semiconductor region (26) formed in the first conductive type semiconductor layer and a contact region (AP) for electrically connecting the first semiconductor region to a line. At least one second unit cell includes a second conductive type second semiconductor region (16) formed in the first conductive type semiconductor layer and a contact region (CP) for electrically connecting the second semiconductor region to a line. An element isolation region (18) is located between the first unit cell and the second unit cell. The first unit cell and the second unit cell act as a diode element (22) in cooperation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figures (APAF 15 (a) and (b)) in view of Dabral et al (US 6,137,143).

In re claim 1, the APAF 15 (b) shows a semiconductor device comprising a first conductive type semiconductor layer (130), at least one first unit cell including a first conductive type first semiconductor region (112) formed in the first conductive type semiconductor layer, and at least one second unit cell includes a second conductive type second semiconductor region (122) formed in the first conductive type semiconductor layer. An element isolation region (132) is located between the first unit cell and the second unit cell. The first unit cell and the second unit cell act as a diode element (140) in cooperation. Although it is well known in the art that semiconductor regions have contacts for electrically connecting said regions to a line, the APAF 15(b) does not specifically show those contact regions. However, Dabral shows (fig. 4) contacts (130 and 140) made to the n-type and p-type regions (125,135, and 145) to dissipate charge to a suitable power supply and to link the diode to a performance circuit (col. 5, lines 42-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the diode regions of the APAF by

adding contacts to the n and p-type regions as taught by Dabral to dissipate charge to a suitable power supply and link the diode to a performance circuit.

In re claim 2, Dabral et al. shows (figs. 4 and 5) that the at least one first unit cell (125) is a plurality of first unit cells and the at least one second unit cell (135) is a plurality of a second unit cells.

In re claim 3, Dabral et al. discloses (col. 5, lines 6-19) that a dimension that defines a size of each of the first semiconductor region (125) and the second semiconductor region (135) is substantially a same as a minimum dimension that is allowed by a design rule for the semiconductor device.

In re claim 4, Dabral et al. shows (figs. 4 and 5) each of the first semiconductor region (125) and the second semiconductor region (135) viewed from a normal line direction is substantially square in shape.

In re claim 5, Dabral et al. shows (figs. 8 and 9) the first unit cells (125) and the second unit cells (135) are arranged in a checkered pattern in the first conductive type semiconductor layer.

In re claim 8, Dabral et al. shows (figs. 8 and 9) a plurality of second unit cells (135) are formed in the first semiconductor region (160) of one first unit cell.

In re claim 13, Dabral et al. shows (fig. 3) an analog circuit section (115) and a digital circuit section (110). The diode element is formed in the analog circuit section. With respect to the limitation that the analog circuit section and the digital circuit section are produced by a CMOS process, that limitation is considered as a product by process limitation. A "product by process" limitation is directed to the product per se, no matter

how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Claims 6, 7, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Figures (APAF 15 (a) and (b)) in view of Dabral et al (US 6,137,143) as applied to claim 1 above, and further in view of Koga (US 5,936,265).

In re claim 6, the APAF in view of Dabral et al. shows (APAF 15 (a)) that the first unit cell (112) and the second unit cell (122) are arranged in the first conductive type semiconductor layer (130) with a predetermined distance (114) to each other. The APAF nor Dabral do not show that on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a

gate electrode structure including at least an insulating layer formed on the cell region and a conductive layer formed on the insulated layer is formed. Koga shows (figs. 11A-12B) a diode element which on an intercell region that is positioned between the first unit cell (205a) and the second unit cell (205b) in the first conductive type semiconductor layer (201), a gate electrode structure (203) including at least an insulating layer (203) formed on the cell region and a conductive layer (204) formed on the insulated layer is formed. With this configuration a diode is formed in which a tunnel current is controlled by the gate to ultimately increase the read speed of a transistor or reduce power consumption (col. 6, lines 15-24). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the diode of the APAF and Dabral by adding a gate between the diode elements as taught by Koga to control the tunnel current of the diode, thereby increasing a read time of a transistor or reducing power consumption during standby mode.

In re claim 7, Koga shows (figs 11A) that a gate line (204a) electrically connects to the gate electrode structure.

In re claim 12, Koga shows (figs. 19A-20B) an embodiment of the invention in which the first conductive type semiconductor layer is formed on an insulating layer.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Figures (APAF 15 (a) and (b)) in view of Dabral et al (US 6,137,143) as applied to claim 1 above, and further in view of Lee et al. (US 4,884,238).

In re claims 9 and 11, the APAF in view of Dabral shows (APAF 15 (a)) shows that the first type semiconductor layer (130) is formed on a second semiconductor layer but does not disclose the specific conductivity type. It is well known in the art that various layers of differing conductivity types are formed on each other. However, Lee et al. shows (fig. 2A) a diode (18) having a second conductive type semiconductor layer (30), wherein a first conductive type semiconductor layer (32',17) is formed on the second conductive type semiconductor layer. The second conducive type semiconductor layer is a semiconductor substrate and the first conductor type semiconductor layer is a well region formed in the semiconductor substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of the APAF and Dabral by adding a second conductivity type because Lee teaches that it is common in the art to do so.

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
February 3, 2005

TOM THOMAS
SUPERVISORY PATENT EXAMINER